REMARKS

Claims 6-10 are pending in this application. Claims 6-10 have been amended. No new matter has been added. Reconsideration and allowance of the present application are respectfully requested.

Claims 7-10 were objected to because of an informality. Applicants have amended the dependency of claims 7-10 accordingly.

Claims 6-8 were rejected under 35 USC 103(a) as unpatentable over Baliga U.S. Patent No. 4,443,931 ("Baliga '931"), Fragapane European Patent Pub. No. 1,058,316 and Baliga U.S. Patent Pub. No. 2004/0099905 ("Baliga '905"). Claims 9 and 10 were similarly rejected under 35 USC 103(a) as unpatentable over Baliga '931, Fragapane, Baliga '905 and two other references. Applicants respectfully traverse these rejections.

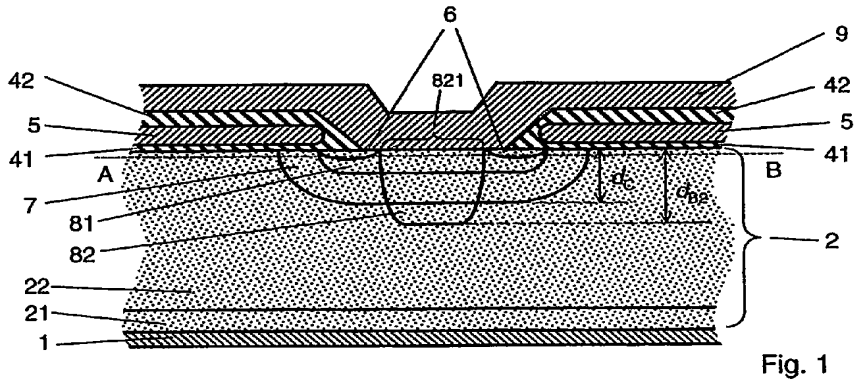

Fig. 1

Applicants' Fig. 1, shown above, displays a cross section of an embodiment of an insulated gate bipolar transistor (IGBT). A bottom metallization layer 1 is disposed on a bottom surface of a silicon semiconductor substrate 2. A p doped emitter layer 21 is disposed in the semiconductor substrate 2 and adjoins the bottom surface. Adjoining the emitter layer 21 is an n doped drift region 22. A gate oxide

film 41 with a contact opening is disposed on the top surface of the semiconductor substrate 2.

A polysilicon gate electrode 5 is formed on top of the gate oxide film 41 and covered by a silicon oxide insulation layer 42. A p doped channel region 7 is disposed in the drift region 22 and adjoins the top surface underneath the contact opening and underneath part of the gate oxide film 41. Disposed in the channel region 7 are one or more n+ doped source regions 6 that delimit a base contact area 821. A top metallization layer 9 covers the oxide insulation layer 42 and the contact opening. In an on-state of the IGBT, an electrically conducting channel is formed underneath the gate oxide film 41 between the one or more source regions 6 and the drift region 22.

A first p^+ doped base region 81 is disposed in the channel region 7 so that it encloses the one or more source regions 6, but does not adjoin the top surface underneath the gate oxide film 41. In other words, the one or more source regions 6, the first base region 81 and the channel region 7 form at least one common boundary line on the top surface of the semiconductor substrate 2.

A second p^+ doped base region 82 is disposed in the semiconductor substrate underneath the base contact region. This second base region 82 is narrower and deeper than the first base region 81, so that the first and the second base regions partially overlap one another.

Laterally confining the second base region 82 to a region underneath the base contact area 821 ensures that an avalanche point, i.e., a location of the highest electric field during turn-off, on a first p-n-junction between the channel region 7 and the drift region 22, is more concentrated away from a periphery of channel region 7,

resulting in most of the avalanche-generated holes not entering the cell via the channel, which would cause early latch-up. As shown in Fig 1, base region 82 does not extend laterally or overlap the two source regions 6

Applicants' claim 6 recites an insulated gate bipolar transistor comprising a semiconductor substrate having a top and a bottom surface and a gate insulation film formed on the top surface. The gate insulation film comprises at least one contact opening.

The semiconductor substrate comprises an emitter layer of first conductivity type adjoining the bottom surface, a drift region of second conductivity type adjoining the emitter layer, a channel region of first conductivity type with a doping concentration p_C formed in the drift region underneath the contact opening and underneath part of the gate insulation film, one or more source regions of second conductivity type disposed in the channel region and delimiting a base contact area, a gate electrode formed on the gate insulation film, a bottom metallization layer formed on the bottom surface and a top metallization layer covering the contact opening and being contacted by one or more source regions.

A first base region of first conductivity type with a doping concentration p_{B1} is disposed in the channel region so that it encompasses the one or more source regions. At least one common boundary line on the top surface is formed by the first base region, the one or more source regions and the channel region on the top surface. The doping concentration p_{B1} of the first base region is higher than the doping concentration p_C of the channel region.

A second base region with a doping concentration p_{B2} of first conductivity type is laterally confined in the semiconductor substrate to a region underneath the base

contact area so that it partially overlaps with the channel region and with the first base region.

The doping concentration p_{B2} of the second base region is higher than the doping concentration p_C of the channel region.

To make claim 6 clear, Applicants have amended it to explicitly recite "a second base region with a doping concentration p_{B2} of first conductivity type is laterally confined in the semiconductor substrate underneath the base contact area so that it partially overlaps with the channel region and with the first base region." Support for this amendment may be found, for example, on page 5, lines 24-25 of Applicants' specification. There, Applicants explain that the lateral confinement of the second base region to a region underneath the base contact area means that the second base region does not extend into or overlap with the source regions.

The claim 6 combination of elements is neither disclosed nor suggested by Baliga '931, Fragapane and Baliga '905, viewed alone or in combination. For example, according to the Action, Baliga '931 discloses a channel region 34 with a doping concentration "p." Baliga's region 28, which the Action equates to Applicants' first base region, is not disposed in the channel region as recited in the claims, but extends to a greater depth than the channel region. It also does not have a common boundary line on the top surface between the first base region, source region and the channel region, as recited in the claims.

However, Baliga '931 shows region 28, which is arranged underneath the base contact area and which overlaps with the channel region. The dose concentration of this second base region is higher than that of the channel region. Although Baliga's region 28 (the second base region) is arranged below the base

contact region, it is not laterally confined to the region underneath the base contact region, but further extends below the source regions 36. As discussed above, Applicants' second base contact region, according to claim 6, is confined to the area underneath the base contact area, i.e., an area delimited by the source regions (see also, for example, Applicants' description on page 4, lines 28-29 and Fig. 1). Therefore, Baliga '931 does not show all of the features for which it is cited.

Fragapane does not compensate for the deficiencies noted above in Baliga '931. Additionally, Fragapane only shows a first base region.

Regarding Baliga '905, Applicants respectfully disagree that this reference shows a semiconductor device similar to Applicants' claimed combination. Baliga '905 is another type of semiconductor device (MOSFET) with an n+ type drain region 406 (i.e., a first conductivity type) instead of an emitter layer of the second conductivity type. As such, Baliga '905 is not analogous to an insulated gate bipolar transistor as claimed by Applicants.

Moreover, Baliga's regions 412, which the Examiner asserts are similar to the second base region of Applicants' claim 6, are not confined to a region underneath the base contact region. These regions are not in contact with the top metallization layer. Instead, Baliga's source regions 416 are arranged above the regions 412. Thus, Baliga's regions 412 are not equivalent to the first base regions, because they do not encompass the source regions.

Therefore, the combination constructed by the Examiner would not have resulted in the claimed device, nor would a person of ordinary skill in the art have been motivated to combine these documents in the manner suggested by the Examiner.

Accordingly, independent claim 6 is allowable. Claims 7-10, which depend directly from claim 6, are also allowable.

Conclusion

For the reasons set forth above, Applicants respectfully request allowance of the pending claims. In the event that there are any questions, the Examiner is respectfully requested to telephone Applicants' undersigned representative so that prosecution of the application may be expedited.

If additional fees are required for any reason, please charge Deposit Account No. 02-4800 the necessary amount.

Respectfully submitted,

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